Laboratory 2

(Due date: **002/003**: February 3rd, **004**: February 4th, **006**: February 5th)

OBJECTIVES

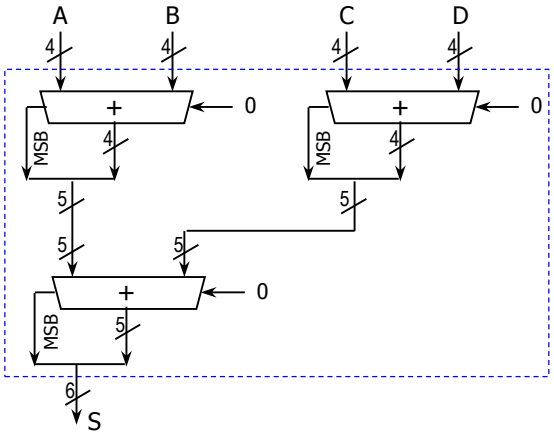
- ✓ Use the Structural Description on VHDL.
- ✓ Test arithmetic circuits on an FPGA.

VHDL CODING

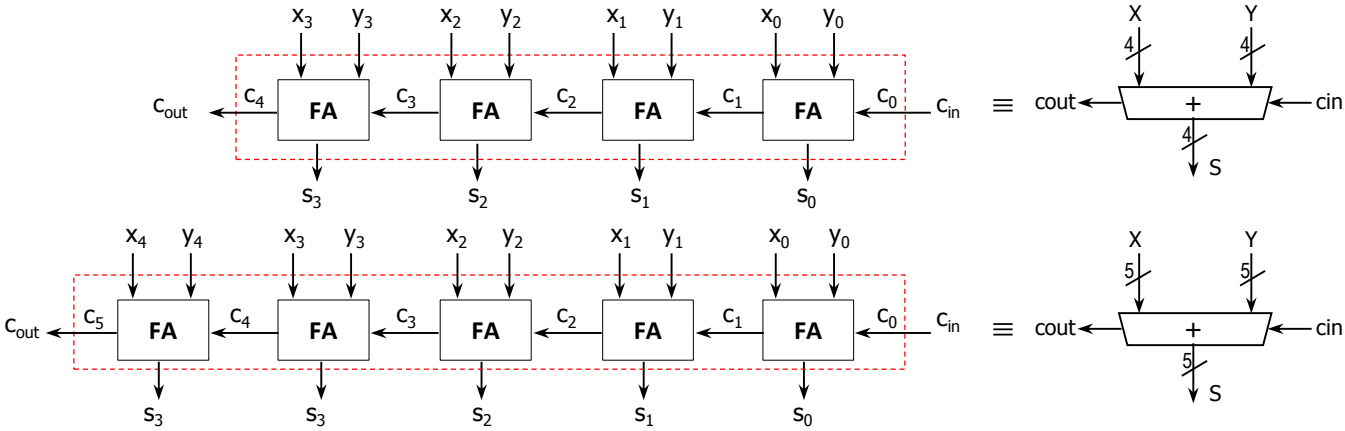
- ✓ Refer to the Tutorial: VHDL for FPGAs for a list of examples.

FIRST ACTIVITY (100/100)

- **PROBLEM**: Addition of four 4-bit unsigned numbers. The addition result requires 6 bits. This circuit can be built out of two 4-bit adders and one 5-bit adder as depicted in the figure ⇒

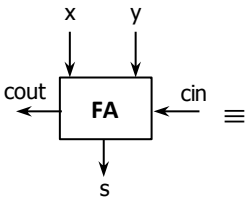


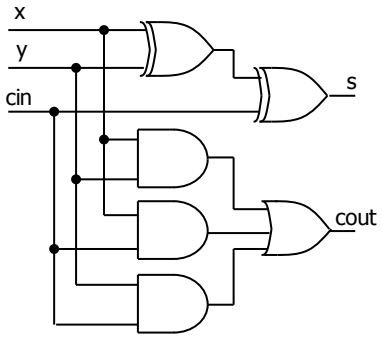
- The figure below depicts the internal architecture of the 4-bit adder and the 5-bit adder. The full adder circuit is also shown.



- ✓ **NEXYS A7-50T**: Create a new Vivado Project. Select the **XC750T-1CSG324 Artix-7 FPGA** device.
- ✓ Write the VHDL code for the Adder of four 4-bit unsigned numbers. Use the Structural Description: Create a separate file for the Full Adder, the 4-bit adder, the 5-bit adder, and the top file (Adder of 4 4-bit numbers).
- ✓ Write the VHDL testbench to test the circuit to test the following cases:
  - ♦ **A**=0x8, **B**=0xE, **C**=0xF, **D**=0x9 → S=101110
  - ♦ **A**=0xF, **B**=0xE, **C**=0x7, **D**=0x3 → S=100111
  - ♦ **A**=0xA, **B**=0x6, **C**=0x4, **D**=0x8 → S=011100

FULL ADDER





- ✓ Perform Behavioral Simulation* and Timing Simulation of your design. **Demonstrate this to your TA**.
  * It is very useful to include internal signals: a) SCOPE: testbench → UUT. b) OBJECTS → Signal(s) → Add to Wave Window.
- ✓ I/O Assignment: Create the XDC file. Nexys A7-50T: Use SW15-SW0 for the inputs, and LED5-LED0 for the outputs.
- ✓ Generate and download the bitstream on the FPGA and test. **Demonstrate this to your TA**.

- Submit (as a .zip file) the five generated files: VHDL code (4 files), VHDL testbench, and XDC file to Moodle (an assignment will be created). DO NOT submit the whole Vivado Project.

TA signature: _____ **Date:** _____

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